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ENERGY AND RADIO SCIENCE

Power Analysis for Automated Adapted Reconfigurable OFDM Transmitter

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Adaptive Modulation, OFDM, Partial Reconfiguration, Power Consumption
Modulation Adaptative, OFDM, Reconfiguration Partielle, Consommation d'Energie

Abstract

The Orthogonal Frequency Division Multiplexing (OFDM) technique is the core of most recent generations of wireless communication systems. This popular technique is found in most smart phones and embedded systems. For these advanced systems, power has been the main subject of interest in the context of Green technologies. To improve the performance of the communication systems in fading wireless channels, researchers have proposed new techniques and methodologies. Adaptive modulation is one of these techniques. In parallel with these new communication schemes, circuit architectures have also greatly evolved. For example, Field Programmable Gate Arrays (FPGAs) are now suitable for implementing the physical layer of wireless systems. This is made possible thanks to their high level of performance, flexibility, and bit level programming. In these devices, the Dynamic Partial Reconfiguration (DPR) concept constitutes a promising technique for reconfiguring only a specific area within the circuit. This technique offers efficient resource utilization, reduced power consumption and permits optimizing the configuration time. Also, the DPR concept provides flexibility in updating design for reconfigurable systems. In our system, we will apply the DPR concept automatically for an adapted OFDM system and evaluate the impact of applying this technique on the power consumption of the system.

La technique (OFDM) (Orthogonal Frequency Division Multiplexing) est au cœur de la plupart des systèmes de communication sans fil tels que le Wifi, le LTE, etc. Pour améliorer les performances des systèmes de communication vis-à-vis des perturbations et des interférences inhérents aux canaux sans fil, les chercheurs ont proposé de nouvelles techniques et méthodologies. La modulation adaptative, corrélée à l'OFDM, est une de ces techniques. Parallèlement à ces nouveaux systèmes de communication, les architectures des circuits embarqués ont également beaucoup évoluées. Par exemple, les circuits programmables (FPGA) sont aujourd'hui adaptés pour la mise en œuvre de la couche physique des systèmes sans fil. Ceci est rendu possible grâce à leur haut niveau de performance, de flexibilité, et la possibilité de les programmer au niveau bit. Dans ces dispositifs, le concept de reconfiguration dynamique partielle (RDP) constitue une technique prometteuse permettant de reconfigurer seulement une zone spécifique à l'intérieur du circuit. Cette technique permet une utilisation efficace des ressources, de diminuer la consommation d'énergie globale et d''optimiser le temps de configuration. En outre, le concept de RDP fournit la flexibilité dans la mise à jour de systèmes reconfigurables. Dans notre système, nous allons appliquer le concept de RDP pour un système OFDM et évaluer l'impact de cette technique sur la consommation d'énergie du système global.

Introduction

First introduced in the 1950's, the OFDM [1] constitutes a very popular modulation scheme allowing a high data rate transmission over wireless mediums. It has become the core of most 4G fixed and mobile wireless communication systems (LTE, WIFI, WIMAX, …).

In order to improve the performance of the OFDM systems with respect to the channel conditions, the adaptive modulation technique has been proposed in [2]. It consists in changing the constellation scheme (for example, to switch from a 4QAM to a 64QAM modulation). This is done according to the Signal to Noise Ratio (SNR) of the received signal, which reflects the status of the channel. In this case, authors in [2] have shown that the overall Bit Error Rate (BER) is improved and that the throughput performance of the OFDM system is increased.

A basic OFDM transmitter/receiver system consists of the following core blocks: encoder/decoder, modulator/demodulator, FFT/IFFT (Fast Fourier Transform/Inverse Fast Fourier Transform), estimator and equalizer in the receiver. In order to provide a large bandwidth and a high performance, these types of blocks should be implemented

on high performance hardware chips. Today, FPGAs are considered as a valuable alternative to their ASICs counterparts. They provide more flexibility, large bandwidth and are appropriate for signal processing applications. FPGAs are also more advantageous to implement OFDM systems than Digital Signal Processors due to their intrinsic parallel hardware architecture.
To apply the adaptive modulation technique on an OFDM system, a classic approach on FPGA device may involve a complete reconfiguration with a new bit-stream. In this case, the whole system is reconfigured whereas only one block of the chain has to be modified. This is obviously considered as time wasting and power consuming. DPR is a technique in the FPGA domain that enables reconfiguring a specific block while the remaining blocks of the system are still running. In our case, we apply DPR on the modulation block in the transmitter while the other blocks of the OFDM system keep operating without any interruption.
Furthermore, with the evolution of the embedded systems and smart phones, the power has become an important issue that needs to be taken into consideration. This point will be also analyzed.
In this paper, we benefit from the DPR technique to implement the adaptive modulation technique in the OFDM transmitter chain. The designed system is implemented on a ZedBoard that features a Xilinx Zynq 7000 SoC with an embedded ARM processor. In particular, we focus on analyzing the impact of applying the DPR concept on the power consumption of the system.

1. Partial Reconfiguration on SoC

1.1. Partial Reconfiguration

Partial Reconfiguration is an interesting feature that has been made available in some FPGA systems. It provides the ability to reconfigure a subset of logic elements in the FPGA system. The main idea of DPR is to reconfigure the function of specific blocks within the system while the remaining blocks keep operating without any interruption. The blocks of the system that can be reconfigured during run time are called reconfigurable modules whereas blocks with no changes are called static modules.
In addition to providing more flexibility; one of the benefits of partial reconfiguration is the cost reduction that is obtained by applying multiple functions on the same FPGA and then switching functionality on demand. It allows reducing resources used on the same FPGA since only one block with multiple functions is implemented rather than having multiple blocks running concurrently. This point is illustrated in Figure 1.

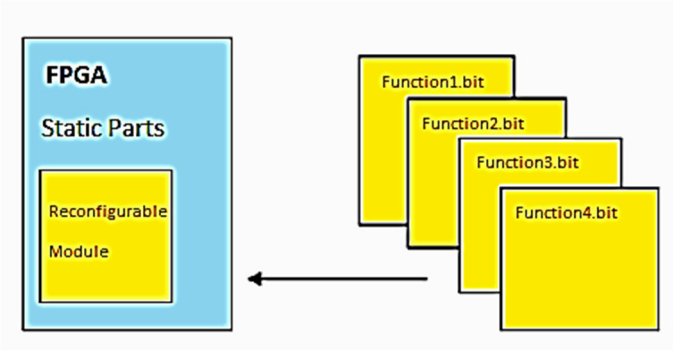

Figure 1. Partial Reconfiguration on FPGA example

Another benefit of DPR consists in reducing the power consumption. This is achieved by sending partial bit-streams to modify a block of the system instead of sending full a bitstream when one block only has to be reconfigured. The authors in [2], [3], [4] have benefited from DPR to propose low power reconfigurable systems for Software Defined Radio (SDR) and Cognitive Radio (CR) applications. The power consumed for the reconfiguration of a part of the communication chain is reduced by applying DPR on the needed module only instead of reconfiguring the full system. In this case the bits streams transferred are minimized and power consumption is reduced. Those works were proposed for SDR and CR systems in which it is always needed to reconfigure part of the communication system.
In our case, we will enable the dynamic partial reconfiguration during runtime according to a decision made by an algorithm implemented on the Processing System (PS). Thus, the impact of applying the DPR concept on the system is taken into consideration. Furthermore, the number of implemented blocks is reduced when the DPR concept is applied. This will reduce the power consumed by the circuit.

1.2. SoC Architecture

The Zynq-7000 SoC is a new technology which consists in integrating both PS and Programmable Logic (PL) into the same chip. A high speed connection is achieved using the Advanced Extensible Interface (AXI) interface interconnection. A simplified model for the SoC architecture is shown in Figure 2.
The PL which is equivalent to a classic FPGA fabric is ideal for implementing high speed logic arithmetic and data flow subsystems. On the other hand, the PS supports software algorithms and operating systems. As a result, the users can

benefit from SoC designs to implement Hardware/Software systems, where the hardware design and architecture are implemented on the PL and the software runs in the PS with a high speed connection between the two parts [5].
The Zynq 7000 proposed by Xilinx is a SoC device whose architecture consists of a dual–core ARM Cortex A9 processor and an Artix-7 or Kintex-7 FPGA fabric [7].

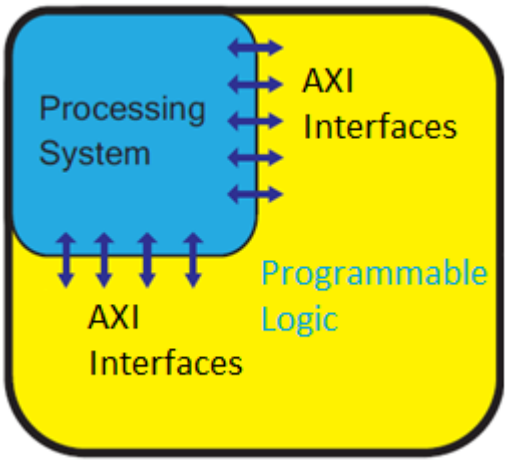

Figure 2. A simplified model of the SoC architecture

2. System Design and Implementation

The OFDM technique divides high data rate streams into multiple low data rate ones, in the frequency domain. Then each stream is modulated and transmitted over multiple orthogonal subcarriers. Adaptive modulation for OFDM systems is a transmission technique that has been proposed to set the best constellation scheme according to the channel conditions, for each sub-channel in order to improve the system performance. Setting the best constellation provides the ability to fully exploit the radio channel and reduce the cost per a transmitted bit in a communication system. The OFDM transmitter chain sequential blocks are: the encoder block, the modulation block, the mapper block, and the IFFT block. In case of applying adaptive modulation technique there are two ways to implement the modulator block: the first one consists in applying the DPR concept (Figure 3) while the second one is based on a switching block implementing all the modulation schemes as shown in Figure 4.

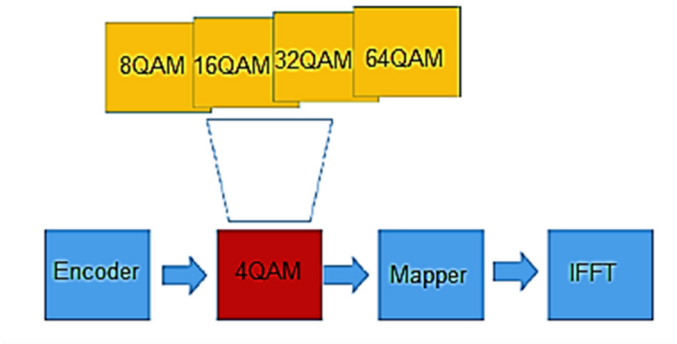

Figure 3. Adapted OFDM Tranmitter design DPR

In case of applying DPR concept we will need to implement only one block of the modulation scheme, and then reconfigure it with another scheme according to the SNR value of the channel. On the other hand, in case of not applying the DPR concept, we need to implement five modulation schemes (in our scenario). A multiplexer is also needed to switch to the selected modulation block. Five versions of a wrapper (called “control_Fifo_mem”) between the encoder and the modulation block are also implemented with another multiplexer to switch between the selected wrapper.

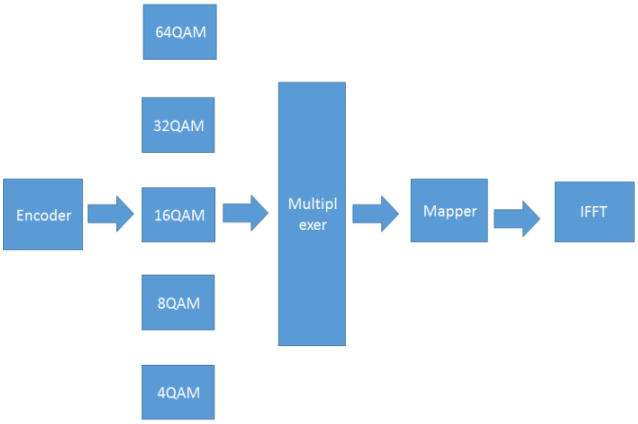

Figure 4. Adapted OFDM Transmitter design without DPR

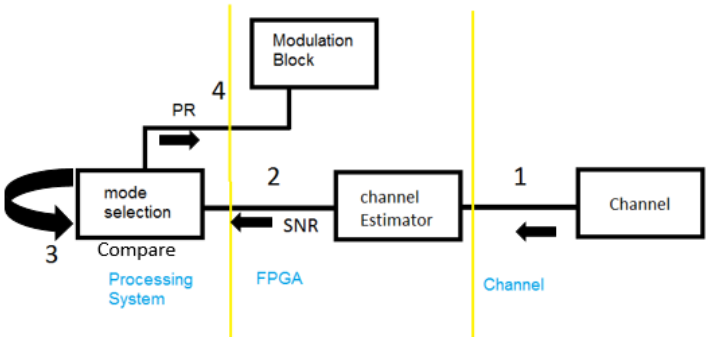

Figure 5. Block Diagram for Applying adaptive Modulation

As described in Figure 4, the Signal to Noise Ratio (SNR) of the received signal is evaluated by the channel estimator block. The received signal is affected by the channel fading and the white Gaussian noise (WGN). The channel estimator provides the SNR value to the decision system on the PS. Based on this information, the PS selects the best modulation scheme to be applied for the transmission. As a result, DPR is applied to the modulation block in the FPGA.

3. System configuration

The parameters used in the transmitter are defined in Table 1.

Parameters	Scenario
Modulation	QAM4,QAM8,QAM16,QAM32,QAM64
(I)FFT Length	256
Cyclic Prefix Length	32
Encoder	3GPP LTE Turbo Encoder 1/3
Frame	1 OFDM pilot + 10 OFDM data symbols
FPGA	Zynq-7000 xc7z020
Clock	200 MHZ

Table 1. Transmitter Parameters

We consider 5 modulation schemes in our scenario as shown in Table 1, and the system runs at 200 MHZ on the Zynq-7000 xc7z020.

4. Power Results

The power consumed by the FPGA chip is the sum of the static and dynamic power. The static power is mainly due to the transistor leakage. It occurs even when the transistor is logically "off". The dynamic power is the sum of transient power consumption and capacitive load power consumption. The transient power consumption represents the amount of power consumed when the device changes logic states, i.e. "0" bit to "1" bit or vice versa. The capacitive load power consumption represents the power used to charge the load capacitance.

There are 3 possible ways to compute power consumed on FPGA:

1- Concept phase: A rough estimate of power can be calculated based on estimates of logic capacity and activity rates.
2- Design phase: Power can be calculated more accurately based on detailed information about how the design is implemented in the FPGA.
3- System Integration phase: Power is calculated in a lab environment.

In our case, we will use the Xpower Analyzer, a design phase analyzer, to estimate the static and dynamic power consumption.

The power results for four scenarios of the circuit are calculated by the software and presented in Table 2. Table 3 presents the results for the modulation blocks and associated control only.

Table 4, Table 5, Table 6 show the results for full OFDM chain scenario. Multi-QAM in Table 5 represents all the possible configurations, from QAM4 up to QAM64. For the control block, Total Control represents all the control according to the modulation.

Block	**Total on chip (W)**	**Total without IO's (W)**	**Dynamic Power (W)**
Control_fifo_mem	0.117	0.115	0.00022
QAM	0.134	0.115	0.00024
Total	**0.251**	**0.230**	**0.00046**

Table 2. Power Results for independent blocks with DPR

Block	**Total on chip (W)**	**Total without IO's (W)**	**Dynamic Power (W)**
Multi.Control_fifo	0.127	0.118	0.00164
Multi_QAM	0.146	0.121	0.00345
Total	**0.273**	**0.239**	**0.00509**

Table 3. Power Results for independent blocks without DPR

	Logic Power (mW)	**Signal Power (mW)**	**Total (mW)**
QAM	0. 01	0. 05	0. 06
Control_fifo mem	0. 02	0. 04	0. 06
Total	**0. 03**	**0. 09**	**0. 12**

Table 4. Power Results for QAM and Control blocks in full OFDM chain with DPR

	Logic Power (W)	**Signal Power (W)**	**Total (W)**
Total Control (5 blocks +Multiplexer)	0.40	0.72	0.00112
Total MultiQAM (5 blocks +Multiplexer)	1.00	0.70	0.00197
TOTAL	**1.40**	**1.41**	**0.00281**

Table 5. Power Results for total control and QAM blocks in no DPR case

	Total on chip (W)	**Dynamic Power (W)**
Circuit Design with No DPR	0.246	0.04448
Circuit Design with DPR	0.242	0.03615

Table 6. Power Results for Full OFDM chain

When applying the DPR concept during system design, the number of blocks running at the same time is reduced. Thus, as it can be noticed from the results presented above, this approach results in reducing the power consumption on the chip. The static power consumption is related to the internal architecture of the FPGA and is therefore not affected by the design change. On the other hand, as results show, the dynamic power consumption is reduced when applying the DPR concept. The results presented in Table 6 show a 1.6% reduction rate of the total power on chip and a 18.7% reduction rate in dynamic power.

Conclusion

In this paper, we propose a SoC system design implemented on ARM-FPGA platform that provides the intelligence of applying the partial reconfiguration technique on adapted reconfigurable OFDM transmitter. The power consumption is calculated and analyzed to determine the impact of applying DPR concept on the proposed design. In addition to the advantages of the adaptive modulation technique in reducing the total power consumption, an additional power reduction is achieved due to applying the DPR concept.

Citations

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